Course Title	**Computer and Network Architecture I**				
Course Code	**CSC202**				
Course Type	**Compulsory**				
Level	BSc/1st Cycle				
Year / Semester	2nd /3rd				
Teacher's Name	Prof. George Dekoulis				
ECTS	7.5	Lectures / week	3 hours	Laboratories / week	2 hours
Course Purpose and Objectives	To introduce computing students to computer architecture and organization.				
Learning Outcomes	By the end of this course students should: • Explain the architecture and flow of information in the Von Neumann machine • Use digital circuits to design the basic units of a CPU, including buses, register files, ALU and control unit. • Describe the operation and characteristics of main memory and bulk storage, design memory modules using RAM and ROM devices, and explain the function and design of memory hierarchy including caches and virtual memory. • Describe the operation and characteristics of main memory and bulk storage, design memory modules using RAM and ROM devices, and explain the function and design of memory hierarchy including caches and virtual memory. • Describe the operation and characteristics of input/output peripheral devices and explain how data is transferred from/to peripheral devices using handshaking, polling, interrupts and DMA. • Implement the basic units of a CPU using VHDL, simulate them, download them on FPGA boards and test their operation.				
Prerequisites	CSC107	Required			
Course Content	• **Introduction to computer architecture:** Hardware level of a computer, instruction cycle, flow of information at the register level. Relation between machine language, assembly language and high level languages. • **Registers:** Internal structure of registers, register transfer operations and micro-operations. Multiplexer and bus-based transfers in multiple register systems. • **Sequencing and control:** Algorithmic state machines, ASM charts, and timing considerations. Control unit implementation, hardwired control and microprogrammed control. • **CPU design basics:** Datapaths, register files, ALU, shift and rotate circuits. Control signals and control words. Instruction Set Architectures, instruction formats and instruction decoding.				

<table>
<tr><td></td><td>

- **Memory basics:** Internal structure of semiconductor memory devices, signals and basic characteristics. Types of memory devices, ROM (masked, programmable, flash) and RAM (dynamic and static). Memory expansion, memory address map.
- **Memory organization:** Memory hierarchy, auxiliary memory, main memory, and cache. Main memory speed characteristics and the locality principle. Cache memory organization, replacement and write policies.
- **Input/Output organization:** Overview of peripheral devices, interfacing and synchronization. Synchronous and asynchronous buses. Handshaking, polling, interrupts and Direct Memory Access. Isolated I/O and memory mapped I/O.
- **Laboratory Work:** Individual or small group experiments performed with the use of common FPGA boards and VHDL. Experiments include the design and analysis of the basic units of a typical CPU such as register files, ALUs and control circuits.

</td></tr>
<tr><td>Teaching Methodology</td><td>

In the Classroom: Lecturers make use of whiteboards, flipcharts, overhead projector, video material and power point presentations. Students are supplied with handouts on extra or relevant material. One Personal Computer Labs equipped with Multimedia PCs of the latest technology with the required software, scanners, printers and LCD-Projectors, satisfy the classes' requirements. All PCs are connected to the Internet, through a Broad Band High speed permanent connection using cable technology.

Web Supported Learning: All the teaching material and the Lecturer's presentations are uploaded on the electronic learning platform of the college as a supporting studying tool.

Guest Speakers / Visits: External visits to agencies or relevant industry/subject related organizations are arranged. Guest speakers that are experts in their field are invited to address the students. Students are also encouraged to visit industry players and familiarize themselves with the profession they have chosen.

Teaching Methods: Lectures, presentations, videos, problem and case study discussion, discussion on relevant articles, independent and private study, preparation of projects, fieldwork and group work.

</td></tr>
<tr><td>Bibliography</td><td>

Required Bibliography:

<table>
<tr><th></th><th>Author(s)</th><th>Title</th><th>Publisher/Year</th><th>Edition</th><th>ISBN</th></tr>
<tr><td>1</td><td>David A Patterson and John L Hennessy</td><td>Computer Organization and Design MIPS Edition: The Hardware / Software Interface</td><td>Morgan Kaufmann Publishers / 2020</td><td>6th</td><td>978-0128201091</td></tr>
<tr><td>2</td><td>Brock J. LaMeres</td><td>Introduction to Logic Circuits & Logic Design with VHDL</td><td>Springer/2019</td><td>2nd</td><td>978-3-030-12489-2</td></tr>
</table>

</td></tr>
</table>

3	George Dekoulis	Laboratory Manual	AUCY 2020	1	-

Recommended Further Bibliography:

	Author(s)	Title	Publisher/Year	Edition	ISBN
1	M. Mano	Logic and Computer Design Fundamentals	Pearson International / 2015	5th	978-1292096070
2	Richard E. Haskell and Darrin M. Hanna	Introduction to Digital Design Using Digilent FPGA Boards	LBE Books/2019	1st	978-0980133769
3	Sanjay Churiwala	Designing with Xilinx® FPGAs: Using Vivado	Springer/2017	1st	978-3-319-42437-8
4	Richard E. Haskell and Darrin M. Hanna	Digital Design Using Digilent FPGA Boards: VHDL / Vivado Edition	LBE Books/2019	1st	978-0982497081
5	Andrzej J. Gapinski	Digital Electronics with DIGILENT BASYS 2 & 3 FPGA Boards: Implementation of Combinational and Sequential Logic Circuits using Digilent BASYS 2 & BASYS 3 Boards with Xilinx FPGAs	LAP/2018	1st	978-6139929764

Assessment

The final course grade is made up of:

Coursework 40%

Final Examination 60%

Final Examination marks constitute 60% of the final semester mark, while Midterm Examinations and assignments (when applicable) constitute the 40% and participation,

The pass mark is set at 50%.

	The Midterm examinations are based on material covered during a given period and are set towards the end of November in the case of Fall semesters, the end of March in the case of Spring semesters, and the end of July in the case of summer sessions. These take place during lesson time and take no more than two study periods to complete. Final examinations are based on material covered throughout the semester. The dates for these are set down on the academic calendar. The Final Examinations have duration of three hours for Diplomas, Bachelor Degrees and Master Degrees. Final examination marks are combined with the marks from the Midterm examinations, participation and assignments (when applicable) to produce the final mark for the semester.
Language	**ENGLISH**