AMERICAN UNIVERSITY
OF CYPRUS

Course Code MH362	**Course Name** Digital Systems 2	**ECTS Credit** 7.5
Pre-Requisite CSC202	**Course Type** Major Elective	**Language of Instruction** English
Year of Study 4th / 7th	**Level of Course** BSc/1st Cycle	**Mode of Delivery** On Campus

Course Objectives:

To introduce students to advanced topic in digital systems design. Design synchronous sequential circuits using techniques such as state diagrams, state equations, and ASM charts. PLD and hardware description languages.

Learning Outcomes:

By the end of this course students should be able to:

- Explain the role of EDA tools for ASIC/VLSI design
- Describe and evaluate the characteristics of ASIC technologies, PLDs FPGAs and HDLs.
- Design and analyse the operation of hazard free asynchronous and synchronous digital systems using ASMs.
- Implement Mealy and Moore ASMs using PROMs, Multiplexers, PLDs, FPLAs and FPGAs.
- Develop VHDL descriptions of digital systems and implement them on FPGA boards for functional testing and verification.

Teaching Methodology:

In the Classroom: Lecturers make use of whiteboards, flipcharts, overhead projector, video material and power point presentations. Students are supplied with handouts on extra or relevant material. One Personal Computer Labs equipped with Multimedia PCs of the latest technology with the required software, scanners, printers and LCD-Projectors, satisfy the classes' requirements. All PCs are connected to the Internet, through a Broad Band High speed permanent connection using cable technology.

Web Supported Learning: All the teaching material and the Lecturer's presentations are uploaded on the electronic learning platform of the college as a supporting studying tool.

Guest Speakers / Visits: External visits to agencies or relevant industry/subject related organizations are arranged. Guest speakers that are experts in their field are invited to address the students. Students are also encouraged to visit industry players and familiarize themselves with the profession they have chosen.

Teaching Methods: Lectures, presentations, videos, problem and case study discussion, discussion on relevant articles, independent and private study, preparation of projects, fieldwork and group work.

Course Content

• **ASIC Architectures and Design Routes:** EDA tools for ASICs. Semi-custom / full custom ASICs. Gate Array, Standard Cell, Full Custom. CMOS/BI-CMOS technologies. PLDs and FPGAs. VHDL.

• **Digital Systems Design – ASMs:** ASMs, Mealy and Moore machines. ASM Charts. VEM minimization. Minimization and realization of IFL/OFL. State machines using PROMs and Multiplexers. PLDs. State machines using FPLAs. Timing Considerations. Glitch suppression techniques. Asynchronous input systems. Selection of an implementation route – economic factors, volumes, time-scales etc. Project management.

• **VHDL:** Top-Down Design. File Organization. Design Examples. Structural Design Versus Behavioral Design. Mixed Level Modeling. VHDL. Primitives. State System. Signal Queues and Delta Times. Sequential Statements. Concurrent Statements. Procedures. Functions. Advanced Topics in VHDL design.

• **Design for Test in ASIC/VLSI Devices:** Testing, verification and production. Component, board level testing and burn-in testing. Testability and design for test (DFT). Ad-hoc methods, structured DFT, built-in test methods, signature analysis.

• **Laboratory Work:** Individual assignments are based on using VHDL, FPGA implementation and testing using the analogous instrumentation.

Assessment Methods:

The final course grade is made up of:

Coursework

Final Examination

Final Examination marks constitute 60% of the final semester mark, while Midterm Examinations and assignments (when applicable) constitute the 40% and participation,

The pass mark is set at 50%

The Midterm examinations are based on material covered during a given period and are set towards the end of November in the case of Fall semesters, the end of March in the case of Spring semesters, and the end of July in the case of summer sessions.

These take place during lesson time and take no more than two study periods to complete.

Final examinations are based on material covered throughout the semester.The dates for these are set down on the academic calendar. The Final Examinations have duration of three hours for Diplomas, Bachelor Degrees and Master Degrees.

Final examination marks are combined with the marks from the Midterm examinations, participation and assignments (when applicable) to produce the final mark for the semester.

Required Textbooks/Reading:

Required Bibliography:

Title	**Author(s)**	**Publisher**	**Year**
Introduction to Logic Circuits & Logic Design with VHDL	Brock J. LaMeres	Springer/2019	2019
Laboratory Manual	George Dekoulis	AUCY 2020	2020

Recommended Further Bibliography:

Title	**Author(s)**	**Publisher**	**Year**

Logic and Computer Design Fundamentals	M. Mano	Pearson International	2015
Computer Organization and Design MIPS Edition: The Hardware / Software Interface	David A Patterson and John L Hennessy	Morgan Kaufmann Publishers	2020
Introduction to Digital Design Using Digilent FPGA Boards	Richard E. Haskell and Darrin M. Hanna	LBE Books	2019
Designing with Xilinx® FPGAs: Using Vivado	Sanjay Churiwala	Springer	2017
Digital Design Using Digilent FPGA Boards: VHDL / Vivado Edition	Richard E. Haskell and Darrin M. Hanna	LBE Books	2019
Digital Electronics with DIGILENT BASYS 2 & 3 FPGA Boards: Implementation of Combinational and Sequential Logic Circuits using Digilent BASYS 2 & BASYS 3 Boards with Xilinx FPGAs	Andrzej J. Gapinski	LAP	2018