AMERICAN UNIVERSITY
OF CYPRUS

Course Code	Course Name	ECTS Credit
CSC202	Computer Architecture I	7.5
Pre-Requisite	**Course Type**	**Language of Instruction**
CSC107	Compulsory	English
Year of Study	**Level of Course**	**Mode of Delivery**
2nd /3rd	BSc/1st Cycle	On Campus

Course Objectives:

To introduce computing students to computer architecture and organization.

Learning Outcomes

By the end of this course students should:

- Explain the architecture and flow of information in the Von Neumann machine
- Use digital circuits to design the basic units of a CPU, including buses, register files, ALU and control unit.
- Describe the operation and characteristics of main memory and bulk storage, design memory modules using RAM and ROM devices, and explain the function and design of memory hierarchy including caches and virtual memory.
- Describe the operation and characteristics of main memory and bulk storage, design memory modules using RAM and ROM devices, and explain the function and design of memory hierarchy including caches and virtual memory.
- Describe the operation and characteristics of input, output peripheral devices and explain how data is transferred from/to peripheral devices using handshaking, polling, interrupts and DMA.
- Implement the basic units of a CPU using VHDL, simulate them download them on FPGA boards and test their operation.

Teaching Methodology:

In the Classroom: Lecturers make use of whiteboards, flipcharts, overhead projector, video material and power point presentations. Students are supplied with handouts on extra or relevant material. One personal Computer Labs equipped with Multimedia PCs of the latest technology with the required software, scanners, printers and LCD-Projectors, satisfy the classes' requirements. All PCs are connected to the Internet, through a Broad Band High speed permanent connection using cable technology.

Web Supported Learning: All the teaching material and the Lecturer's presentations are uploaded on the electronic learning platform of the college as a supporting studying tool.

Guest Speakers / Visits: External visits to agencies or relevant industry/subject related organizations are arranged. Guest speakers that are experts in their field are invited to address the students. Students are also encouraged to visit industry players and familiarize themselves with the profession they have chosen.

Teaching Methods: Lectures, presentations, videos, problem and case study discussion, discussion on relevant articles, independent and private study, preparation of projects, fieldwork and group work.

Course Content

- **Introduction to computer architecture:** Hardware level of a computer, instruction cycle, flow of information at the register level. Relation between machine language, assembly language and high level languages.

- **Registers:** Internal structure of registers, register transfer operations and micro-operations. Multiplexer and bus-based transfers in multiple register systems.

- **Sequencing and control:** Algorithmic state machines, ASM charts, and timing considerations. Control unit implementation, hardwired control and microprogrammed control.

- **CPU design basics:** Data paths, register files, ALU, shift and rotate circuits. Control signals and control words. Instruction Set Architectures, instruction formats and instruction decoding.

- **Memory basics**: Internal structure of semiconductor memory devices, signals and basic characteristics. Types of memory devices, ROM (masked, programmable, flash) and RAM (dynamic and static). Memory expansion, memory address map.

- **Memory organization**: Memory hierarchy, auxiliary memory, main memory, and cache. Main memory speed characteristics and the locality principle. Cache memory organization, replacement and write policies.

- **Input/Output organization**: Overview of peripheral devices, interfacing and synchronization. Synchronous and asynchronous buses. Handshaking, polling, interrupts and Direct Memory Access. Isolated I/O and memory mapped I/O.

- **Laboratory Work**: Individual or small group experiments performed with the use of common FPGA boards and VHDL. Experiments include the design and analysis of the basic units of a typical CPU such as register files, ALUs and control circuits.

Assessment Methods:

The final course grade is made up of:

Coursework

Final Examination

Final Examination marks constitute 60% of the final semester mark, while Midterm Examinations and assignments (when applicable) constitute the 40% and participation,

The pass mark is set at 50%

The Midterm examinations are based on material covered during a given period and are set towards the end of November in the case of Fall semesters, the end of March in the case of Spring semesters, and the end of July in the case of summer sessions.

These take place during lesson time and take no more than two study periods to complete.

Final examinations are based on material covered throughout the semester. The dates for these are set down on the academic calendar. The Final Examinations have duration of three hours for Diplomas, Bachelor Degrees and Master Degrees.

Final examination marks are combined with the marks from the Midterm examinations, participation and assignments (when applicable) to produce the final mark for the semester.

Required Textbooks/Reading:

Title	Author(s)	Publisher	Year
Computer Organization and Design MIPS Edition: The Hardware / Software Interface	David A Patterson and John L Hennessy	Morgan Kaufmann Publishers / 2020	2020
Introduction to Logic Circuits & Logic Design with VHDL	Brock J. LaMeres	Springer/2019	2019
Laboratory Manual	George Dekoulis	AUCY 2020	2020

Recommended Further Bibliography:

Title	Author(s)	Publisher	Year
Logic and Computer Design Fundamentals	M. Mano	Pearson International /2015	2015
Introduction to Digital Design Using Digilent FPGA Boards	Richard E. Haskell and Darrin M. Hanna	LBE Books / 2019	2019
Designing with Xilinx FPGAs: Using Vivado	Sanjay Churiwala	Springer/2017	2017
Digital Design Using Digilent FPGA Boards: VHDL / Vivado Edition	Richard E. Haskell and Darrin M. Hanna	LBE BOOKS/2019	2019
Digital Electronics with DIGILENT BASYS 2 & 3 FPGA Boards: Implementation of Combinational and Sequential Logic Circuits using Digilent BASYS 2 & BASYS 3 Boards with Xilinx FPGAs	Andrzej J. Gapinski	LAP/2018	2018